Voltage Ramp Stress (VRS) based test methods for reliability characterization of Hf-base high-k/metal gate stacks for CMOS technologies

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The transistor technology for CMOS applications has been rapidly shifting from transistors with conventional SiO2/poly-Si gate stacks to transistors with high-k/metal gate (HKMG) stacks, and processors with these new fully deposited gate stacks are already used in commercial products. The HKMG stacks allow for further oxide thickness scaling, enabling gate length scaling according to the semiconductor roadmap map and in addition provide significant gate leakage advantages over conventionally scaled stacks.

The trends of reliability parameters – such as Time Dependent Dielectric Breakdown (TDBB), Negative Bias Temperature Instability (NBTI), Positive Bias Temperature Instability (PBTI) -for FETs with SiO2/SiON gate dielectrics are well studied since oxide scaling has continuously evolved over the last 3 decades with gradual changes to the basic Si/SiON/poly-Si gate stack structure. Therefore, early reliability screening was typically not a priority.

With the introduction of high-k dielectrics and metal gates, a radical transition to new materials has occurred, rendering the applicability of the historical knowledge base less useful. For these reasons, it is important to systematically evaluate the gate stack reliability already during the early gate stack development phase as well as during the device optimization phase which often results in substantial changes to the gate stack properties as performance in optimized and matched. Additionally, as the gate stack are scaling down from one technology node to the next – requiring thinner interlayer (IL) and/or thinner high-k dielectric – a reduction in the reliability margins of scald stacks is to be expected. In order to avoid gate stack optimization into a parameter space where reliability specs can no longer be met, systematic, continuous and rapid reliability monitoring during the whole development and optimization phase is desirable.

To meet these requirements, novel Voltage-Ramp test methodology for Dielectric Breakdown (VBD, Breakdown Voltage, [1]), and for NBTI (Negative Bias Temperature Instability) and PBTI (Positive Bias Temperature Instability) [2] have been recently proposed and we have used these methods systematically for HKMG transistor and MOS capacitor characterization.

The purpose of this contribution is three fold.

1. We introduce the Voltage-Ramp based Stress (VRS) methodology and discuss the advantages of these VRS based methods over conventional Constant Voltage Stress (CVS) methods. In a nutshell, with a ramp test it is guaranteed that an appropriate stress voltage condition – at which an easily measurable shift in the device parameters is induced - can always be reached without any uncertainties in the test time. Therefore, one single test with fixed test parameters can be used for many technologies with widely different gate stack requirements, such as high performance, low power, SG and EG oxides. For VRS no a priori gate stack information is needed to extract the reliability parameters.

Such tests are perfectly sited for inline application where the test time is of primary concern. Since the gate voltage is varied at a constant rate, the test time can be accurately set by the ramp rate, overcoming well known timing limitations of a constant voltage methodology for such tests.

2. We will review recent publications on VRS applications and demonstrate both, theoretically and experimentally, that the reliability parameters obtained from these VRS tests are equivalent to the parameters measured and used in conventional Reliability Technology Qualifications based on CVS methodologies. Therefore, the parameters obtained during the development phase with the VRS tests can be used as zero order input parameters for final reliability qualifications with the CVS methods, which will remain the primary vehicle for final reliability qualifications.

3. Finally, we will discuss some reliability trends with gate stack scaling for more advanced technology nodes as they are emerging from these VRS tests. We will show that these tests also provide insights into the physical mechanisms dictating these trends. TDBB and NBTI/PBTI margins are in general observed to shrink with both IL and HK scaling. It is shown that interlayer scaling leads to significant reductions of the breakdown voltage, $V_{BD}$.[3]. It is shown that NBTI is a field driven phenomenon and is largely determined by the IL thickness and chemical composition, whereas PBTI is observed to be primarily a gate current driven phenomenon, depending primarily on the defect properties of the HK layer in the dual layer gate stack. The oxide interlayer acts primarily as a current modulator. For PBTI, the understanding of transient charging will become increasingly important. All of these statements will be documented and illustrated with recent examples of breakdown voltage (VBD), NBTI and PBTI VRS screening results and literature data [2-4].