Selective etching of SiGe for removal of dummy layers in fully silicided gate architectures

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ABSTRACT

Selective removal of SiGe is widely used to produce advanced device structures, such as silicon on nothing (SON) [1,2] or silicon quantum wires (SQWR) [3]. In a new approach SiGe is used as a dummy material for fully silicided (FUSI) gates [4]. Before depositing the metal used for silicidation, e.g. Ni, the poly-crystalline SiGe has to be removed selectively to the exposed oxide and nitride of the spacers and to the exposed Si, crystalline or polycrystalline. Afterwards the metal will be deposited and during the annealing step the exposed silicon will react with the metal to form a metal silicide. HNO$_3$/HF/CH$_3$COOH and H$_2$O$_2$/HF/CH$_3$COOH mixtures are known to be able to remove SiGe selectively to Si [2, 5]. It was found that the doping had a pronounced effect on the selectivity. B-doping did not have a significant effect on the etch rate of poly-Si with HNO$_3$/HF/CH$_3$COOH. However as soon as the poly-Si was doped with As or with P, the etch rate increased drastically. On the other hand the etch rate of SiGe was much less affected which led to a loss in selectivity, especially for As- and P-doped materials (Fig. 1). While the required selectivity vs. silicon nitride could be achieved and silicon oxide selectivity was acceptable, the lack of selectivity to doped polysilicon forced the evaluation of SC1 mixtures [6]. Figure 3 shows the selectivity on a SEZ spin processor with an APM 1:1:4 at elevated temperatures. With this chemistry, FUSI devices could be produced (Fig. 4). Additional improvements in selectivity could be achieved via the use of Si$_{0.7}$Ge$_{0.3}$.

REFERENCE

[1] Lee, et al., to be published in the proceedings of UCPSS 2004